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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,910	DHANOA, KULWINDER	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-8 and 11-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-8 and 11-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
11/3/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/22/2006 has been entered.

Response to Arguments

2. Applicant's arguments filed 08/22/2006 have been fully considered but they are not persuasive. Currently, claims 3-4 and 9-10 are canceled and claims 1-2, 5-8 and 11-17 are pending for examination.

3. In responding to applicant's argument regarding independent claim 1 rejected under 35 U.S.C. 103(a) that Gray and Becker do not teach all the claimed limitations, because Gray and Becker do teach the limitation that prevents the need for an additional request to go back and get the data for the end of the request, thereby increase the available bandwidth, as stated on page 7, 1st paragraph. Applicant's arguments have fully been considered, but are found not to be persuasive.

Please note that the features upon which applicant relies (i.e., prevents the need for an additional request to go back and get the data for the end of the request) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

4. In responding to applicant's argument regarding independent claim 1 rejected under 35 U.S.C. 103(a) that the Gray reference does not teach the claimed limitation " ... a memory interface including a plurality of buffers ... " as stated on page 8, 1st paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

As discussed in the preceding Final office action (page 3, section 6), the memory interface disclosed by Gray comprises the DMA engine (Gray, Fig. 3, ref. 200) and the memory interface (Gray, Fig. 3, ref. 270), wherein Gray's memory interface (Gray, Fig. 3, ref. 200, 270) includes a plurality buffers (e.g. device buffers 204, 206, 208, 209 of Fig. 3); and further more, Gray also discloses the various blocks can be integrated (Gray, col. 7, ll. 56-64).

5. In responding to applicant's argument regarding independent claim 1 rejected under 35 U.S.C. 103(a) that Gray does not teach or suggest the control logic for assigning multiple burst for a single request to a plurality of buffers in the memory interface; Gray does not teach or suggest the claimed limitation of different buffer for

different portions of a single request from a single device; and Becker does not teach or suggest the claimed limitation that data needed for the beginning and end of a single request are stored concurrently in a single buffer and the wrapping request, as stated on page 8, 2nd paragraph to page 9 1st paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Please note the claimed limitation of independent claim 1 stated " ... wherein, for a wrapping memory access request requiring multiple buffers, data required a beginning and an end of the wrapping memory access request are assigned to a single respective buffer by the control logic and stored in the single respective buffer by the memory interface," and as discussed in the preceding Final office action (pages 3-5 in section 6), said claimed limitation is rejected by the combined teachings of Gray and Becker under 35 U.S.C. 103(a); therefore, please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

More specifically regarding the combined teachings of Gray and Becker; Gray teaches the memory interface (Fig. 3, ref..220, 270); receiving memory access request, which utilized a single respective buffer (e.g. single respective device buffer) (Fig. 4, ref. 204, 206, 208, 209) for storing data to be transferred by the memory interface (col. 8, ll. 10-22), wherein data for the first device (Fig. 3, ref. 221) is stored in the first device buffer (Fig. 3, ref. 204), data for the second device (Fig. 3, ref. 222) is stored in the second device buffer (Fig. 3, ref. 206) and so on; and the DMA engine (i.e. control logic)

maintains the buffered data in the single respective device buffer (Fig. 3, ref. 204, 206, 208, 209) as DMA engine is responsible for providing data to each device and for monitoring the remaining data in the corresponding device buffers, and further more, the DMA engine provide arbitration functionality to the devices as well as the memory (col. 2, ll. 47-56), therefore, it would have been obvious for the DMA engine to implement the assigning of the single respective device buffer to be utilized for the corresponding device.

Gray does not teach a wrapping memory access request requiring multiple buffers, data required a beginning and an end of the wrapping memory access request.

Becker teaches DMA data transferring utilizing a circular memory (Fig. 2A-2B) implemented for buffering a steam of data (col. 4, ll. 32-41 and col. 8, l. 65 to col. 9, l. 12); wherein the transferring of the stream of data utilizes multiple blocks of the circular buffer, therefore implementing the transferring of multiple data burst, as each burst is stored in one of the multiple blocks of the circular buffer (Fig. 4C-4D); and wherein the transferring of the stream of data access the first frame and the last frame on the single circular buffer, resulting in the wrapping around of the single circular buffer (Fig. 4C-4D), as the ES memory buffer (Fig. 2A and Fig. 4C) is utilized for the inputting data stream (col. 4, ll. 59-65) and the AS buffer (Fig. 2B and Fig. 4D) is utilized for outputting data stream (col. 5, ll. 6-19), therefore, the data request associated to the transferring of the stream of data would be a wrapped memory access request.

By combining Becker's circular buffer for buffering the transfer of multiple data bursts into each of Gray's single respective device buffers (i.e. each of the single

respective device buffer is further configured to have the circular buffer with multiple blocks for the transferring of the respective stream of data), the resulting combination of the references further teaches the receiving of the wrapping memory access request requiring the circular buffer's multiple blocks in the single respective device buffer, wherein the transferring of data access the first block (i.e. beginning) and the last block (i.e. end) of the circular buffer in the single respective device buffer; and the assigning of the corresponding single respective device buffer is implemented by the DNA engine (i.e. control logic) and the data is stored into the single respective device buffer by the memory interface.

Please also note, the same grounds of rejection utilizing the same art was discussed in detail in the preceding Final office action. As applicant has also stated, the combination of Becker with Gray implemented by combining Becker's circular buffer ***into each*** of Gray's device buffer (i.e. single respective device buffers) (Applicant's response, page 9, 2nd paragraph), therefore Gray's first single respective device buffer (Gray, Fig.3, ref. 204) is implemented with Becker's circular buffer, Gray's second single respective device buffer (Gray, Fig.3, ref. 206) is implemented with Becker's circular buffer, and so on for each of Gray's corresponding single device buffer (Gray, Fig. 3, ref. 204, 206, 208, 209), resulting in each one of Gray's single respective device buffers would be implemented with Becker's circular buffer; and the data request associated with the data transferring that resulted in the wrapped around of the circular buffer in the corresponding single respective device buffer would be the wrapped memory access request.

6. In responding to applicant's argument regarding independent claim 1 rejected under 35 U.S.C. 103(a) that there would be no motivation to combine Gray and Becker because the applicant appears to argue that the references are not analogues, as stated on page 9, 2nd paragraph. Applicant's arguments have fully been considered, but are found not to be persuasive.

In response to applicant's argument that Gray and Becker are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Gray and Becker teaching both corresponds to DMA data transferring (Gray, Fig. 1-2 and Becker, col. 2, ll. 23-31), wherein Gray further teaches the implementation in a multi-processor system (Gray, col. 5, ll. 36-40) and Becker's DMA data transferring is implement in the corresponding multi-processor system (Becker, col. 2, ll. 23-31).

7. As applicant applies similar argument stated for independent claim 1 to independent claims 7 and 13 due to recitation of similar claimed limitations, examiner would also applies similar responses as discussed in detail above to independent claims 7 and 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 7-8, 13-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) in view of Becker et al. (US Patent 6,950,884).

9. As per claims 1, 7 and 13, Gray teaches a memory controller system, method and programmable logical device, comprising:

at least one bus interface (devices interface 250 of Fig. 2-3), each bus interface being for connection to at least one respective device (device 221-224 of Fig. 3) for receiving memory access requests (col. 8, ll. 52-63);

a memory interface (Fig. 2-3, ref. 200, 270), for connection to a memory device (Fig. 2-3, ref. 210) over a memory bus (Fig. 2-3), wherein the memory interface utilize a list structure to provide the scheduling of data storing in response to the memory access request (Fig. 5-6 and col. 9, ll.13-22);

a plurality of buffers (Fig. 3, ref. 202-209) in the memory interface (Fig. 3, ref. 200, 270); and

control logic (DMA engine 200 of Fig. 2), for placing received memory access requests into a queue of memory access requests (col. 10, l. 65 to col. 11, l. 24),

wherein the queue of memory access requests comprising the critical request queue and the non-critical request queue for receiving the respective memory access request,

wherein, in response to a received memory access request requiring data transferring over the memory bus, data is stored in a single respective buffer of said plurality of buffers by the memory interface (col. 8, ll. 10-22), wherein data for the first device (Fig. 3, ref. 221) may be stored in the first device buffer (Fig. 3, ref. 204), data for the second device (Fig. 3, ref. 222) is stored in the second device buffer (Fig. 3, ref. 206) and so on; and

wherein the DMA engine (i.e. control logic) maintains the buffered data in the single respective device buffer (Fig. 3, ref. 204, 206, 208, 209) as DMA engine is responsible for providing data to each device and for monitoring the remaining data in the corresponding device buffers (i.e. each of the single respective device buffer), and further more, the DMA engine provide arbitration functionality to the devices as well as the memory (col. 2, ll. 47-56).

Gray does not expressly teach the memory controller system, method and programmable logical device, comprising:

the DMA engine (i.e. control logic) implementing the assigning function;

wherein the received memory access request requires multiple data bursts; and

wherein, for a wrapping memory access request requiring multiple buffers, data required a beginning and an end of the wrapping memory access request.

Becker teaches a buffer system and method comprising:

a circular memory (Fig. 2A-2B) implemented for buffering a steam of data transferring between two functional units (col. 4, ll. 32-41 and col. 8, l. 65 to col. 9, l. 12);

wherein the transferring of the stream of data utilizes multiple blocks of the circular buffer, therefore implementing the transferring of multiple data burst, as each burst is stored in one of the multiple blocks of the circular buffer (Fig. 4C-4D); and

wherein the transferring of the stream of data the accesses the first frame and the last frame located on the circular buffer, resulting in the wrapping around of the circular buffer (Fig. 4C-4D), as the ES memory buffer (Fig. 2A and Fig. 4C) is utilized for the inputting data stream (col. 4, ll. 59-65) and the AS buffer (Fig. 2B and Fig. 4D) is utilized for outputting data stream (col. 5, ll. 6-19), therefore, the data request associated to the transferring of the stream of data would be a wrapped memory access request.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Becker's circular buffer for buffering the transfer of multiple data bursts into each of Gray's device buffers (i.e. each of the single respective device buffer is further configured to have the circular buffer with multiple blocks for the transferring of the respective stream of data). The resulting combination of the references teaches the memory controller system, method and programmable logical device, comprising:

the DMA engine assigning by allocating the single respective device buffer of the plurality of device buffers in the memory interface in response to the received memory access request, wherein such implementation would have been obvious as the DMA

engine is utilized for receiving the memory access request from the devices, maintaining and monitoring the corresponding device buffers, and implementing arbitration function for the devices and the memory;

implementing the circular buffer in each of the single respective device buffers (Gray, Fig. 3, ref. 204, 206, 208, 209) for the transfer of the data stream for each respective devices;

receiving the memory request requiring multiple blocks of the circular buffer in the single respective device buffer, therefore having multiple data bursts over the memory bus, the DMA engine assigning the single respective device buffer of the plurality of device buffers in the memory interface for each of the multiple data burst, and the memory interface storing each of the multiple data burst in the single respective buffer; and

receiving the wrapping memory access request requiring the circular buffer's multiple blocks in the single respective device buffer, wherein the transferring of data access the first block (i.e. beginning) and the last block (i.e. end) of the circular buffer in the single respective device buffer; and the assigning of the corresponding single respective device buffer is implemented by the DNA engine (i.e. control logic) and the data is stored into the single respective device buffer by the memory interface.

Therefore, it would have been obvious to combine Becker with Gray for the benefit of providing rapid transfer of data and low delay flow coordination between two functional blocks (Becker, col. 1, ll. 54-60).

10. As per claims 2 and 8, Gray and Becker teach all the limitations of claims 1 and 7 as discussed above, Gray further teaches the memory controller system, method and programmable logical device, comprising wherein, when returning data to the respective device from which a memory access request requiring multiple data bursts over the memory bus was received, data is read out from a first part of the single buffer, then data is read out from at least one other of said buffers, then data is read out from a second part of the single buffer (Gray, col. 12, ll. 18-30), wherein the particular device of the plurality of devices (Gray, Fig. 3, ref. 221-224) can make request for data every other cycle, therefore data associated with the first device (Gray, Fig. 3, ref. 221) is read from the associated device buffer (Gray, device buffer 204 of Fig. 3), then data of the second device (Gray, Fig. 3, ref. 222) is read from the associated device buffer (Gray, device buffer 206 of Fig. 3), then returns to the reading the associated device buffer (Gray, device buffer 204 of Fig. 3) of the first device (Gray, Fig. 3, ref. 221).

11. As per claims 14 and 16, Gray and Becker teach all the limitations of claims 1 and 7 as discussed above, where Gray further teach the memory controller system, method and programmable logical device, comprising wherein each of the plurality of buffers is a sub-buffer (e.g. each of the plurality of single respective device buffers) (Gray, Fig. 3, ref. 204, 206, 208, 209) of a larger memory buffer (Gray, Fig. 3, ref. 202) in the memory interface (Gray, Fig. 3, ref. 200, 270).

12. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) and Becker et al. (US Patent 6,950,884), and further in view of Kuronuma et al. (US Patent 6,859,848).

Gray and Becker teach all the limitations of claims 1 and 7 as discussed above, where Gray further teaches the memory controller system, method and programmable logical device, comprising allocating a respective portion of the one of said buffers (Gray, Fig. 3, ref. 204-209) for each of the memory burst (Gray, col. 8, ll. 10-22).

Gray and Becker does not expressly teach the memory controller system, method and programmable logical device, comprising wherein the control logic determines whether a received read access request is a wrapping request which requires multiple memory bursts.

Kuronuma teaches the controlling system and method for sequential access to a SDRAM comprising a detector detecting the number of possible sequential access to the SDRAM associated to a received DMA request (col. 4, ll. 27-44), wherein the detection would determine the number of multiple memory burst required by the received DMA request.

It would have been obvious to one of ordinary skill in this art, at the time when invention was made to include Kuronuma's detection of the number of possible sequential access of the SDRAM into Gray and Becker's control logic. The resulting combination of the references teaches the control logic comprising the detection of the number of sequential access to the memory and the resulting access of the memory would require the wrapping around of the circular memory, therefore, the detection

would be detecting the number of required multiple memory burst accessing the memory resulting in the wrapping around of the circular memory, as the detection associated to the memory access request would be the wrapping memory access request.

Therefore, it would have been obvious to combine Kuronuma with Gray and Becker for the benefit of providing a relative simple configuration for accessing the memory for multiple sequential memory bursts (Kuronuma, col. 4, ll. 15-20).

13. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) and Becker et al. (US Patent 6,950,884), and further in view of "Microsoft Computer Dictionary".

Gray and Becker teach all the limitations of claims 1 and 7 as discussed above.

Gray and Becker does not expressly teach the memory controller system, method and programmable logical device, comprising wherein the memory controller is a SDRAM controller, and said memory interface is suitable for connection to a SDRAM memory device over said memory bus.

"Microsoft Computer Dictionary" teaches the utilization of the SDRAM, wherein it is well known by one skilled in the art that SDRAM is a common type of RAM utilized within the computer system (Page 469).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Microsoft Computer Dictionary's SDRAM into Gray and Becker's memory (Gray, Fig. 3, ref. 210). The resulting combination of the references

teaches the utilization of the SDRAM as the memory (Gray, Fig. 3, ref. 210), therefore the memory controller is a SDRAM memory controller and the memory interface (Gray, Fig. 3, ref. 270) is a SDRAM memory interface capable of coupling to the SDRAM memory over the memory bus.

Therefore, it would have been obvious to combine "Microsoft Computer Dictionary" with Gray and Becker for the benefit of that SDRAM can run at a higher clock speed ("Microsoft Computer Dictionary", Page 469).

14. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) and Becker et al. (US Patent 6,950,884), and further in view of Nguyen et al. (US Patent 5,335,326)

Gray and Becker teach all the limitations of claims 1 and 7 as discussed above.

Gray and Becker does not expressly teach the memory controller system, method and programmable logical device, comprising wherein the control logic is operable to record the value of a pointer indicating the single respective buffer from which data required for the end of the wrapping memory is to be retrieved.

Nguyen teaches a FIFO buffer flow regulation system and method comprising a central control (Fig. 1, ref. 34) utilizing a channel sequence registers (Fig. 2, ref. 74-1, 74-2) comprising the input pointer (Fig. 2, ref. 86-1, 86-2) and the output pointer (Fig. 2, ref. 88-1, 88-2) for pointing to the proper slot for the next input operation and the next output operation respectively (col. 5, ll. 60 to col. 6, ll. 22).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Nguyen's utilization of the plurality of pointers by the central control into Gray and Becker's control logic. The resulting combination of the references teaches the control logic comprising the plurality of pointers pointing to the single respective buffer's circular buffers for the accessing of the first block and the last block on the circular buffer, therefore the control logic would record the pointer values to the last block of the circular buffer as the accessing of the circular buffer results in the wrapping around of the circular buffer.

Therefore, it would have been obvious to combine Nguyen with Gray and Becker for the benefit of proper tracking and control regarding the accessing of the circular buffer (Nguyen, col. 5, ll. 60-66).

Conclusion

All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Please note, as discussed in detail above, that the examiner utilizes the same ground of rejection for claims 1-2, 5-8 and 11-17 with the same art that was applied in the preceding Final office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.K.L.
11/03/2006

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